## System-Wide Roofline Profiling - A Case Study on NERSC's Perlmutter **Supercomputer**

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PMBS24, held in conjunction with SC24 Atland GA November 18, 2024



# How do we describe HPC workloads to help system architects make better design choices?

Top 60 Codes at NERSC; Jan 18 - May 15, 2023



## It is not a simple task

- HPC workloads can be extremely diverse. For example, NERSC hosts:
	- 850 projects
	- o 800 distinct codes
	- 11,000 users  $\rightarrow$  11,000 uses
- Each use-case may have different performance sensitivities.







# How do we describe HPC workloads to help system architects make better design choices?

#### NERSC utilization. Jan 18- May 19, 2023

Top 50 codes, grouped by algorithm similarity



## Current best practice

- Carefully selection of "representative" jobs.
	- o Two benchmarks can represent 60% of the workload !?
	- No information about the remaining workload
- Deep analysis of selected jobs
	- o Analysis is resource intensive
	- $\circ$  Not easily scaled to other jobs.







# How do we describe HPC workloads to help system architects make better design choices?

Top 60 Codes at NERSC; Jan 18 - May 15, 2023



### This work: System-wide sampling

- Limited performance counter selection
- Full coverage of entire workload
- Eliminates selection bias and extrapolation error
- Low sampling rates
- No insight into individual codes
- Limited to simple performance models









### ● System and Monitoring Infrastructure

What is the prevailing floating-point precision used at NERSC?

### ● Roofline Performance Model

Is the performance of NERSC's workload typically bound by FLOPs or bandwidth?

### ● NERSC-10 Benchmarks

How well does this benchmark suite reflect the FLOP/Byte ratio of the workload?







# Perlmutter - an HPE Cray EX System

- 1,536 GPU accelerated nodes
	- 1x AMD Milan CPU
	- 4x NVIDIA A100 GPUs with 40 GB HBM
- 3,072 CPU nodes
	- o 2x AMD Milan CPUs
- Slingshot 11 interconnect
- 35 PB all Flash Lustre file system
- Later added 346 GPU nodes with 80 GB HBM









## Data Acquisition

## Collection Pipeline

- On-node metrics sampled using NVIDIA DCGM (Data Center GPU Manager)
- Cross-system aggregation using LDMS (Lightweight Distributed Metrics System)
- Stored in NERSC's OMNI (Operations Monitoring and Notification Infrastructure)

## Volume

- All 1,536 40GB A100 GPU nodes
- Sampled at 1-second intervals
- Entire month of July, 2024
- $\approx$  16 Billion samples, each corresponds to one GPU-second









## GPU Metrics Collected



Each metric value represents an average over a time interval (i.e. our 1 second sampling period) and is not an instantaneous value.







## What is the prevailing floating-point precision used at NERSC?



Distribution of FLOP types on Perlmutter GPUs

- Double precision (FP64) FLOPS are twice as common as single precision (FP32) FLOPS.
- Half of the FP64 FLOPS run on tensor cores.
	- o All tensor activity attributed to FP64
	- o Tensor cores support TF32, but not FP32
	- o No corresponding non-tensor FP16
- Half precision (FP16) is rarely used









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## Roofline Performance Model

#### Hypothesis

- Kernel performance is limited by either:
	- a) the rate of executing operations, e.g. FLOP/s ("compute-bound"), or b) the rate of transferring operands to the cores ("memory-bound")

#### Processor Characteristics

- Peak floating point performance
- Peak memory bandwidth
- $\bullet \quad \rightarrow$  Attainable Performance Ceiling

#### Kernel Characteristics

• Arithmetic Intensity = Number of FLOPs executed Number of bytes transferred to/from memory

## Kernel Performance

Arithmetic Intensity × Peak Bandwidth,

• Performance = min{

Peak FLOP/s









# Arithmetic intensity distributions are easily computed from DCGM metrics



Arithmetic Intensity (FLOPs/Bytes)







Performance Roofline (TF/s)

# Full-system Arithmetic Intensity Distributions

- $FP32:$ 
	- Almost always memory-bound Median = 0.06 FLOPs/ byte
- FP64:
	- Long tail of high intensity Median = 3.2 FLOPs/byte
- FP64 Tensor:
	- $\circ$  Median = 0.2 (why?!)
- All precisions:
	- The majority of samples have AI values substantially below the machine balance.



## Is the performance of NERSC's workload typically bound by FLOPs or bandwidth?

- Introducing a "pseudo64" FLOP type
	- Needed to compute a compute a single arithmetic intensity from multiple FLOP types
	- $\circ$  FLOPS<sub>Pseudo64</sub> = 1  $\times$  FLOPS<sub>FP64</sub> +  $\frac{1}{2} \times FLOPS$ <sub>FP32</sub> +  $\frac{1}{4}$  X FLOPS<sub>FP16</sub>  $+$  1  $\times$
- FLOPS<br>■ Median pseudo64 Arithmetic Intensity: 7.5 FLOPS/Byte
- On Perlmutter's A100 GPUs, 46% of cycles memory-bound 54% are compute-bound.



Arithmetic Intensity (FP-ops / byte)







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# NERSC-10 Benchmark Suite

- Cross section of NERSC's workload
	- Spans many axes of computational diversity
	- Six GPU codes + two CPU codes
- Profiled configuration
	- "Small" problem size
	- Ran using 4 GPUs on 1 node









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## Diversity of NERSC-10 benchmarks is reflected by their Arithmetic Intensity Distributions



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## How well does the NERSC-10 benchmark suite reflect the FLOP/Byte ratio of the workload?

- Same range of arithmetic intensities
- Same 50/50 balance of memory- and compute bound samples
- Effects of using a finite suite are clearly visible









## **Conclusion**

- First of a kind analysis using full-system sampling to understand the performance characteristics of an entire supercomputer workload, revealing:
	- Distribution of FLOP types: ⅔ FP64, ⅓ FP32, <0.1% FP16
	- Distribution of arithmetic intensities: Median = 7.5 pseudo-64 FLOPs/byte
	- On A100 GPUs, ½ of cycles are memory- bound,  $\frac{1}{2}$  are compute bound.
- The NERSC-10 benchmarks replicate the Perlmutter's overall balance of memory- and compute-bound samples, but the effects of using a finite suite are clearly visible in the shapes of the arithmetic intensity distribution.
- Full-system sampling and traditional performance modeling are complementary approaches to understanding architectural trade-offs.
- 19 Many refinements, extensions & experiments will follow ! • Results show today are preliminary.



https://tinyurl.com/29j93uk3





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## Thank You

This research used resources of the National Energy Research Scientific Computing Center (NERSC), a Department of Energy Office of Science User Facility using NERSC award ASCR-ERCAP0026875. ROR: https://ror.org/05v3mvq14



